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10/606,728	06/26/2003	Brendan K. Bridgford	X-1216 US	5830

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EXAMINER	
RIAD, AMINE	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/606,728	BRIDGFORD, BRENDAN K.	
	Examiner	Art Unit	
	Amine Riad	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 September 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-17* is/are pending in the application.

4a) Of the above claim(s) *12, and 13* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) *1-11 and 14-17* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

Detailed Action

Claims 1-17 have been presented for examination.

Claims 12 and 13 have been cancelled.

Claims 1-8, 9-11,14, 15, 16, and 17 have been rejected.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-8,9,10,14,15,16, and 17 are rejected under 35 U.S.C. 102(b) as being anticipated by Johnson U.S. Patent 5,898,701.

In regard to claims 1, and 16 Johnson discloses a method for debugging a configuration process of a programmable logic device comprising:

- initiating the configuration process for the programmable logic device; (Abstract; "In one embodiment of the present invention, a method for testing a device is described in which a device is instructed in one instruction to receive address information and a first data packet.")
- using boundary scan register for the programmable logic device to capture configuration process signals in the programmable logic device during the configuration process and (Column 2 lines 19-22 & Figure 2; item 212 " Boundary scan register 212 allows testing of board interconnections, testing of typical production defects such as opens and shorts and allows access to component

input and output"); (Abstract; "The device is then instructed to read or capture a second data packet from the address location defined by the address information" and (Column 2; line 21-22)"allows access to component input and output")

- transferring the captured configuration process signals to a configuration analyzer; (Abstract; The second data packet is then output from the device)
- and analyzing the transferred configuration process signals using the configuration analyzer.(Abstract; "The second data packet may then be compared with the first data packet to verify the correct initial programming of the first data packet to verify the correct initial programming of the first data packet at the address location in the device.")

In regard to claim 2, Johnson discloses the method of claim 1 further comprising programming a configuration device coupled to the programmable logic device with a configuration bit stream. (Summary of the invention; "In one embodiment of the present invention, a method for testing a device is described in which a device is instructed in one instruction to receive address information and a first data packet" and (Column 2; lines 2-3 "Control logic 202 receives and interprets the signals on TMS 218 and TCK 220") [the disclosure above proves that the programmable device is coupled to a configuration device])

In regard to claim 3, Johnson discloses the method of claim 2 wherein initiating the configuration process comprises causing the programmable logic device to send normal configuration process signals to the configuration device, thereby causing the

configuration device to provide the configuration bit stream (Summary; "The second data packet is then output from the device. Additionally, the device may be instructed to selectively receive a third data packet and then load the third data packet" [Examiner considers outputting the second set of data to receive a third set of data as an initiation of the configuration process])

In regard to claim 4, Johnson discloses the method of claim 1 wherein initiating the configuration process comprises accessing the programmable logic device through JTAG interface. (Column 5; lines 12-15 "The novel method and apparatus may be implemented with test logic compatible with IEEE Std 1149.1 or with test logic compatible with other standards or architectures.")

In regard to claim 5, Johnson discloses the method of claim 4 further comprising: Executing a SAMPLE/PRELOAD instruction on the programmable logic device; and executing an EXTEST instruction on the programmable logic device. [This is inherent because 1149.1 standard requires that all compliant devices must perform the SAMPLE/PRELOAD and EXTEST instructions]

In regard to claim 6, Johnson discloses the method of claim 5 further comprising executing a BYPASS instruction on a configuration device coupled to the programmable logic device. (Column 2; lines 7-8 "boundary scan register 212 and bypass register 214 are configured to receive input signals from decode control logic 204" [control logic 202 and 204 are coupled to the configuration device as demonstrated before.])

In regard to claim 7, Johnson discloses the method of claim 1 wherein analyzing the transferred configuration process signals comprises comparing the transferred

configuration process signals with expected configuration process signals. (Abstract; "The second data packet may then be compared with the first data packet to verify the correct initial programming of the first data packet to verify the correct initial programming of the first data packet at the address location in the device.")

In regard to claim 8, Johnson discloses the method of claim 7 wherein if the transferred and the expected configuration do not match then correcting the configuration process. (Abstract; "Additionally, the device may be instructed to selectively receive a third data packet and then load the third data packet into the device without overwriting the address information already stored in the device. The first data packet and the address information may be serially shifted into the device.")

In regard to claim 9, Johnson discloses a system comprising:

- a programmable logic device (Figure 1; item 10);
- a configuration device coupled to the programmable (Figure 3; item 218 is the connection point where the device under test couples to the configuration device) logic device for providing a configuration bit stream to the programmable logic device (Column 3; lines 24-26 "In one embodiment of the present invention, a method for testing a device is described in which a device is instructed in one instruction to receive address information and a first data packet.");
- configuration analyzer coupled to the configuration device for driving configuration process signals through the configuration device in single steps, and coupled to the programmable logic device for controlling the I/O pins of the programmable logic device and analyzing configuration process signals stored in

the boundary scan registers of the programmable logic device during the configuration process; (Figure 2; items 106 and 108)

- wherein the programmable logic device, the configuration device and the analyzer form at least part of a JTAG chain. (Figure 2; items 102 and 104)

In regard to claim 10, Johnson discloses the system of claim 9 wherein the configuration device is a nonvolatile memory (Column 3; lines25-26 "The address information and the first data packet are loaded into the device" [Examiner considers that when the data packet is loaded only after it is stored in non-volatile memory, and consequently as demonstrated before the configuration device is a non volatile memory])

In regard to claim 14, Johnson discloses the system of claim 9 wherein the analyzer comprises a computer running a program for analyzing the configuration data (Column 1; lines 14-16 "Various techniques have been developed to enable testing of a device, such as an integrated device, by including test logic into the device itself.")

In regard to claim 15, Johnson discloses the system of claim 14 wherein the analyzer comprises a database of known configuration problems. (Abstract; Examiner considers the second set of data and third set of data when read from the test circuit to constitute a database of known configuration problem)

In regard to claim 17, Johnson discloses a configuration analyzer for debugging a configuration process of a programmable logic device comprising:

- means for stepping through the configuration process; (Abstract; "In one embodiment of the present invention, a method for testing a device is described

in which a device is instructed in one instruction to receive address information and a first data packet.")

- means for capturing configuration process signals received by the programmable logic device at each step; and means for comparing the captured configuration process signals with expected configuration process signals. (Column 2 lines 19-22 & Figure 2; item 212 " Boundary scan register 212 allows testing of board interconnections, testing of typical production defects such as opens and shorts and allows access to component input and output"); (Abstract; "The device is then instructed to read or capture a second data packet from the address location defined by the address information" and (Column 2; line 21-22)"allows access to component input and output")

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Johnson U.S. Patent 5,898,701 in view of Lindholm U.S. Patent 6,553,523.

Johnson discloses a method for debugging a configuration process of a programmable logic device.

Johnson does not disclose that the programmable logic device is a field programmable gate array.

Lindholm teaches that the programmable logic device is a field programmable gate array (Column 7; line 58).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to use the field programmable gate array of Lindholm in the debugging method of Johnson. A person of ordinary skill in the art would have been motivated to use the field programmable gate array of Lindholm because as Lindholm discloses "An example programmable logic device is the field programmable gate array. PLD's such as FPGAs are becoming increasingly popular for use in electronics systems. For example, communications systems employ FPGAs in large measure for their re-programmability. In general, the use of FPGA's continues to grow at a rapid rate because they permit relatively short design cycles, reduce costs through logic consolidation, and offer flexibility in their re-programmability."

Response to Applicant's Arguments

Applicant arguments filed on September 20, 2007 have been fully considered, and are not persuasive.

In regard the first argument, which states, "According to Applicant's claims, the use of the boundary scan register enables verifying a connection to an input/output pin of the programmable logic device coupled to receive configuration process signals at the input output pin. There is no teaching or suggestion in Johnson that a boundary scan register of Johnson is coupled to an input/output pin receiving configuration process signals. In

contrast, Johnson merely teaches that a boundary scan register is coupled to either a test data input signal, a test clock or decoded test mode signal. There is also no teaching or suggestion that the circuit of Johnson enable verifying a connection to an input/output pin of the programmable logic device coupled to receive the configuration process signals" Examiner respectfully disagrees.

Examiner points Applicant to Figure 4. This figure shows clearly that Boundary Scan Register item 312 is coupled to items 318, 320, and 322, which are TMS, TCK, and TDI test data, input signal. Examiner also points Applicant to (Column 3)"In one embodiment of the present invention, a method for testing a device is described in which a device is instructed in one instruction to receive address information and a first data packet. The address information and the first data packet may be selectively passed through a first storage element in to a second storage element. The device is then instructed to read or capture a second data packet from the address location defined by the address information. The second data packet may be compared to the first data packet to verify the initial correct programming." It is clear that it is through item 322, which is test data input signal, or TDI that the two packets (considered as the main part of the configuration process) get inputted to boundary scan register 312. Additionally, Johnson discloses in (Column 2) "Boundary scan register 312 allows testing of board interconnections, testing of typical production defects such as opens, and shorts, and allows access to component inputs and outputs." This passage demonstrates that the present reference enables verifying a connection to an I/O pin.

Applicant argument is not valid.

Contact

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Amine Riad whose telephone number is 571-272-8185. The examiner can normally be reached on 8-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert Beausoliel can be reached on 571-272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

AR
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